UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,427	12/30/2003	Dan M. White	Intel-017PUS	8110

7590 05/04/2007

Daly, Crowley & Mofford, LLP
c/o PortfolioIP
P.O. Box 52050
Minneapolis, MN 55402

EXAMINER	
WU, JUNCHUN	

ART UNIT	PAPER NUMBER
2191	

MAIL DATE	DELIVERY MODE
05/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/748,427	WHITE, DAN M.	
	Examiner	Art Unit	
	Junchun Wu	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *2/23/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-24 are pending in this application.

Claim Rejections - 35 USC § 102

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-5, 7, and 12-15 are rejected under 35 U.S.C. 102(b) as being anticipated by Bade et al. (US Pub. No.20020059054 A1, hereinafter "Bade").

3. Per claim 1

Bade discloses

- A method of displaying embedded firmware program information ([0021] "An integrated design environment (IDE) is disclosed for simulating embedded systems")

Comprising:

- displaying a first screen to interact with a user for high level function selections ([0101] *"As shown in **FIG.**21the IDE preferably has a menu-driven graphical user interface that preferably includes a design window for creating a design with toolbars for accessing functions using a computer mouse or similar interface. The IDE preferably includes a peripheral design editor and simulator that is adapted to permit hardware IP components and processes to be created and linked with other IP components."*).

- displaying a second screen to show hardware resources for a programmable circuit ([0099] *"As shown in **FIGS. 28, 29,** and **37,** the use of an instruction set accurate simulator to model a processor core permits the processor simulator to exchange memory transactions with the hardware partition and to receive interrupts from the hardware partition using APIs linking the hardware partition and the instruction set accurate simulator."*).

- displaying a third screen to show source code for a plurality of source code programs to control the programmable circuit ([0173] *"The IDE preferably features a high-quality C++ code generator, hiding all the details of generating simulation code..."*)

- displaying a fourth screen to show symbolic information associated with the displayed source code ([0104] *"**FIG. 36B** shows an example of a software debugger interface window **3685** superimposed over a design window **3620** of a virtual embedded system." & In Fig. 36B shows the design window 3620 associated with source code that is debugging in debugger window 3620*).

4. Per claim 2

the rejection of claim 1 is incorporated and further, Bade discloses

- displaying source code associated with a symbol selected by the user ([0101]

*"Referring to **FIG. 15**, in a preferred embodiment the graphical object symbols may be selected from a menu **1520**, a textual portion of the object input by the user, and the graphical object connected to other graphical objects using connectors 1505.").*

5. Per claim 3

the rejection of claim 2 is incorporated and further, Bade discloses

- displaying a view source button (*As shown in **FIG**.15 or toolbar shown in **FIG**.25, the button **C** is for generate C++ code*).

6. Per claim 4

the rejection of claim 1 is incorporated and further, Bade discloses

- the symbolic information is associated with one or more of code labels, data labels, data register names, and index register names ([0104] "*Referring to **FIG. 36A**, a software debugger is also preferably included for loading and testing software that is executed on the virtual platform. The software debugger preferably includes means to establish break-points of execution of the software application and to view and modify processor and system resources such as the processor stack, registers, and memory." & The software debugger inherently include source code and data information.*).

7. Per claim 5

the rejection of claim 1 is incorporated and further, Bade discloses

- displaying the symbolic information without typing by the user ([0101] *"Referring to **FIG. 15,** in a preferred embodiment the graphical object symbols may be selected from a menu **1520,** a textual portion of the object input by the user, and the graphical object connected to other graphical objects using connectors 1505."*).

8. Per claim 7

the rejection of claim 1 is incorporated and further, Bade discloses

- displaying a device enabling expansion of the displayed symbolic information ([0129] *"**FIG. 16** shows a Block construct containing a single Process construct, two Block constructs and a Declaration construct." & [0131] "In the example, the interrupt controller waits for an interrupt signal, as sent by one of the two peripheral devices. The Symbol for a Signal-In construct is a rectangle with an arrow pointing inward as either its left or right side."*).

9. Per claim 12

the rejection of claim 1 is incorporated and further, Bade discloses

- the programmable circuit includes a network processor ([0021] *"The IDE includes a graphical user interface and a design language for forming finite state machine models of hardware components that are coupled to processor simulators, preferably instruction set accurate simulators of processor cores."*).

10. Per claim 13

Bade discloses

An embedded firmware development system, comprising:

- a control module to control the system ([0084] *"**FIG. 4A** is a block diagram illustrating major software modules of a preferred embodiment of the IDE. Further details on the interfaces coupling the software modules are described below in more detail. The software modules of IDE may reside on a memory of a computer having a computer processor and memory, such as personal computer or computer coupled to a network server."*)

- a device interface module coupled to the control module to communicate with a device to be programmed by the system ([0086] *"A simulation loader module invokes other IDE modules when a simulation of an embedded system is initiated from GUI module."*).

- an assembler module coupled to the control module to assemble source code ([0145] *"In one embodiment, the models are hand-written CIC++ models for a particular processor core, with assembly routines for the critical portions to improve speed of performance."*).

- a main module coupled to the control module to display a high-level function screen ([0101] *"As shown in **FIG.**21 the IDE preferably has a menu-driven graphical user interface that preferably includes a design window for creating a design with toolbars for accessing functions using a computer mouse or similar interface. The IDE preferably includes a peripheral design editor and simulator that is adapted to permit*

hardware IP components and processes to be created and linked with other IP components.").

- a source module coupled to the control module to display source code for at least two firmware programs ([0085] *"code generator module, and compiler module may be coupled to GUI software module as a hardware design and modeling module for forming a description of the hardware partition of an embedded system."*).

- a hardware resource module coupled to the control module to display hardware resources associated with the device to be programmed ([0085] *"An editor and debugger module, design database module, code generator module, and compiler module may be coupled to GUI software module as a hardware design and modeling module for forming a description of the hardware partition of an embedded system."*).

- a speedbar module coupled to the control module to display symbolic information associated with the source code ([0085] *"a graphical user interface (GUI) software module for a user to interact with IDE"*).

11. Per claim 14

the rejection of claim 13 is incorporated and further, Bade discloses

- the symbolic information includes at least one of code labels, data labels, data

structures, data register names, and index register names ([0104] "*Referring to **FIG. 36A**, a software debugger is also preferably included for loading and testing software that is executed on the virtual platform. The software debugger preferably includes means to establish break-points of execution of the software application and to view and modify processor and system resources such as the processor stack, registers, and memory.*" & *The software debugger inherently include source code and data information.*).

12. Per claim 15

the rejection of claim 13 is incorporated and further, Bade discloses

- the device includes a network processor ([0021] *"The IDE includes a graphical user interface and a design language for forming finite state machine models of hardware components that are coupled to processor simulators, preferably instruction set accurate simulators of processor cores."*).

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 6 and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Bade, in view of Hall et al. (U.S. Patent No. 4,720,778 hereinafter "Hall").

15. Per claim 6

the rejection of claim 1 is incorporated and further, Bade does not disclose

- displaying symbolic information associated with data structures.

But Hall discloses

- displaying symbolic information associated with data structures (col.10 lines 51-56).
- Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify teaching of Bade with the teachings of Hall to include displaying symbolic information associated with data structures in order to generate these symbols and labels in program assembly or compilation can be used directly in defining measurement. These performance measurement capabilities are fundamental to aid the user's verification and validation activities for improved software reliability, as well as in the basic debug process (Hall, col.2 lines 10-20).

16. Per claim 8

the rejection of claim 6 is incorporated and further, Bade does not disclose

- displaying address and value information associated with the data structures.

But Hall discloses

- displaying address and value information associated with the data structures (col.16 lines 56-61 *"The measurement works by setting up the address range comparator*

for recognition over the specified module/line range to drive the count enable signal. Before the measurement is executed, microprocessor loads count mapper, using the line number information found in the compiler database file." & col.14 lines 3-6 *"The trace statements measurement traces statement flow within a single module. The statements are displayed in the order of their execution and variable values are displayed."*).

- Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify teaching of Bade with the teachings of Hall to include displaying address and value information associated with the data structures in order to trace and count the statement flow in one module for the measurement (Hall, col.13 lines 23-25 & col.16 lines 28-30).

17. Claim 9 rejected under 35 U.S.C. 103(a) as being unpatentable over Bade, in view of van Hoff et al. (U.S. Patent No. 5,778,231 hereinafter "Hoff").

18. Per claim 9

the rejection of claim 1 is incorporated and further, Bade does not discloses

- parsing the source code to create a list items for symbols files associated with the source code.

But Hoff discloses

- parsing the source code to create a list items for symbols files associated with the source code (col.2 lines 12-17 *"The inventive compilation method for compiling*

program source code on a computer to generate compiled code includes identifying symbol references in the source code sequentially as the symbolic references occur in the source code, and parsing the code during the compilation to identify each symbol that references another program.'').

- Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify teaching of Bade with the teachings of Hoff to include parsing the source code to create a list items for symbols files associated with the source code in order to identify externally defined symbols so that the compiler can determine whether the symbols is reference to a remotely located file or to a locally stored file. (Hoff, col.5 lines 42-49).

19. Claim 10 rejected under 35 U.S.C. 103(a) as being unpatentable over Bade, in view of Hoff and in further view of Hall.

20. Per claim 10

the rejection of claim 9 is incorporated and further, but Bade and Hoff do not disclose

- outputting symbolic information for a data structure recursively until resultant fields are no longer structures.

However Hall discloses

- outputting symbolic information for a data structure recursively until resultant fields are no longer structures (col.13 lines 36-38 "*Values of important variables can be*

seen at each level of a recursive procedure; this is especially useful if a procedure is stuck in infinite recursion.").

- Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine teachings of Bade and Hoff and further include outputting symbolic information for a data structure recursively until resultant fields are no longer structures by the teachings of Hall in order to trace the values of data at the entry and exit points of procedure. (Hall, col.13 lines 23-24).

21. Claim 11 rejected under 35 U.S.C. 103(a) as being unpatentable over Bade, in view of Smith et al. (U.S. Patent No. 6,311,324 B1 hereinafter "Smith").

22. Per claim 11

- the rejection of claim 1 is incorporated and further, Bade does not disclose.

But Smith discloses

- displaying the symbolic information for particular regions of the source code (col.4 lines 36-39 "*a tuning program proceeds to analyze application code modules to identify critical regions called hotspots, and displays a graphical view of every hotspot in a module*").
- Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify teaching of Bade with the teachings of Smith to include displaying the symbolic information for particular regions of the source code in order to help the user to analyze the region. Once the region has been

identified and analyzed, the program advises the user on how to rewrite the program code to improve the performance of the overall application. (Smith, col.3 lines 4-9).

23. Claims 16-24 are an article comprising a storage medium corresponding to method claims 1-12 respectively, and rejected under the same rational set forth in connection with the rejection of claims 1-12 respectively, as noted above.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junchun Wu whose telephone number is 571-270-1250. The examiner can normally be reached on 8:00-17:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wei Zhen can be reached on 571-272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Junchun Wu

WEI ZHEN
SUPERVISORY PATENT EXAMINER